Question 1:

T / F Name dependencies can be completely eliminated by a hardware mechanism at run-time

Question 2:

T / F Loops with no inter-iteration (loop-carried) dependencies can be executed in parallel.

Question 3:

T / F Data forwarding can resolve all data hazards

Question 4:

T / F Pipelining increases overall instruction throughput but also increases individual instruction latency

Question 5:

Branch, MemWrite and MemRead are control set of

(Memory Access / Instruction Fetch / Execution / Instruction Decode)

Question 6:

Load and store instructions, sum of contents of base register and sign-extended offset is used as

(a register number / a memory address / an operand / operator)

Question 7:

A group of students have been debating the efficiency of five-stage pipeline when one student pointed out that not all instructions are active in every stage of the pipeline. After deciding to ignore the effects of hazards, they made the following five statements. Which ones are correct?

1.Allowing branches, and ALU instructions to take fewer stages than the five required by the load instruction will increase pipeline performance under all circumstances.

2. You cannot make ALU instructions take fewer cycles because of the writeback of the result, but branches can take fewer cycles, so there is some opportunity for improvement.

3. Instead of trying to make instructions take fewer cycles, we should explore making the pipeline longer, so that instructions take more cycles, but the cycles are shorter. This could improve performance.

4. Trying to allow some instructions to take fewer cycles does not help, since the throughput is determined by the clock cycle; the number of pipe stages per instruction affects latency, not throughput.

Question 8:

Predicting branches at runtime by using run-time information, is known as

(Static branch prediction / Stall prediction / Dynamic branch prediction / None of the above)

Question 9:

Ideal CPI (Cycle per Instruction) on a pipelined processor is almost always \_1\_\_.

Question 10:

Simplest Scheme to handle branches is to

(Flush pipeline / Freezing pipeline / Depth of pipeline / Both A and B)